FIG 1

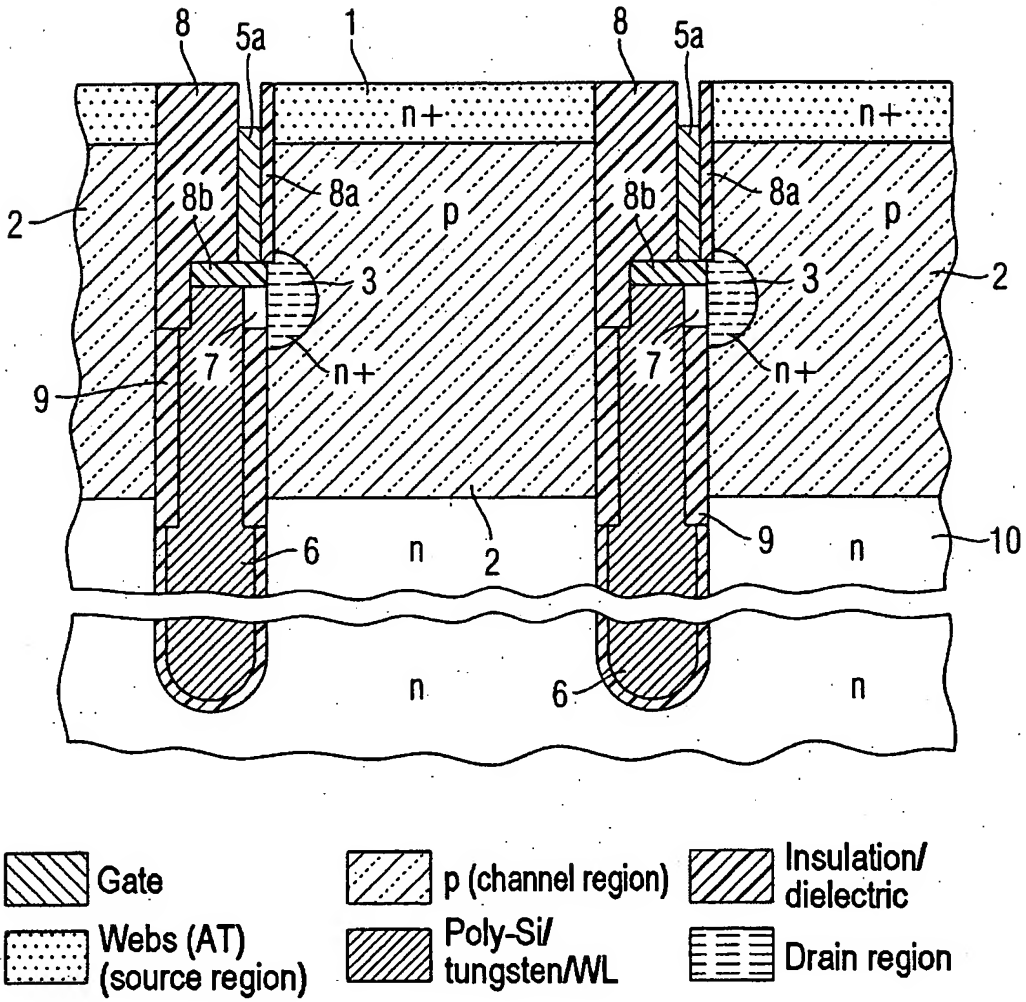

8
5a
1
8
5a
n+
n+
2
8b
8a
p
8b
8a
p
3
3
2
7
7
n+
n+
9
6
n
2
9
n
10
n
6
n
Gate
p (channel region)
Insulation/ dielectric
Webs (AT) (source region)
Poly-Si/ tungsten/WL
Drain region

FIG 2A

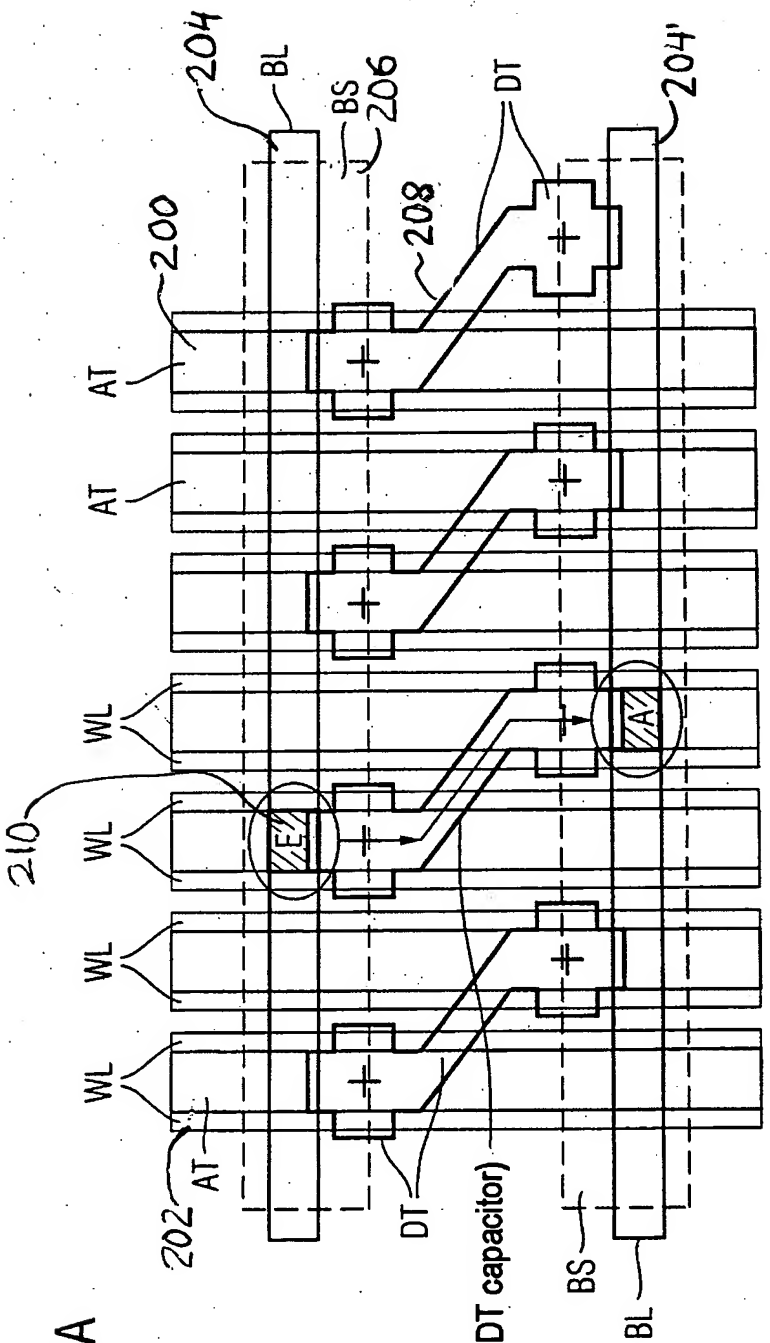

204
BL
BS
206
208
DT
204'
200
AT
AT
WL
WL
WL
WL
210
E
A
202
AT
DT
(DT capacitor)
BS
BL
E: Input through CB to the bit line BL
A: Output through CB to the bit line BL
Buried strip (BS)
Diagonal deep trench DT
CB contacts to the bit line (source contacts)

FIG 2B

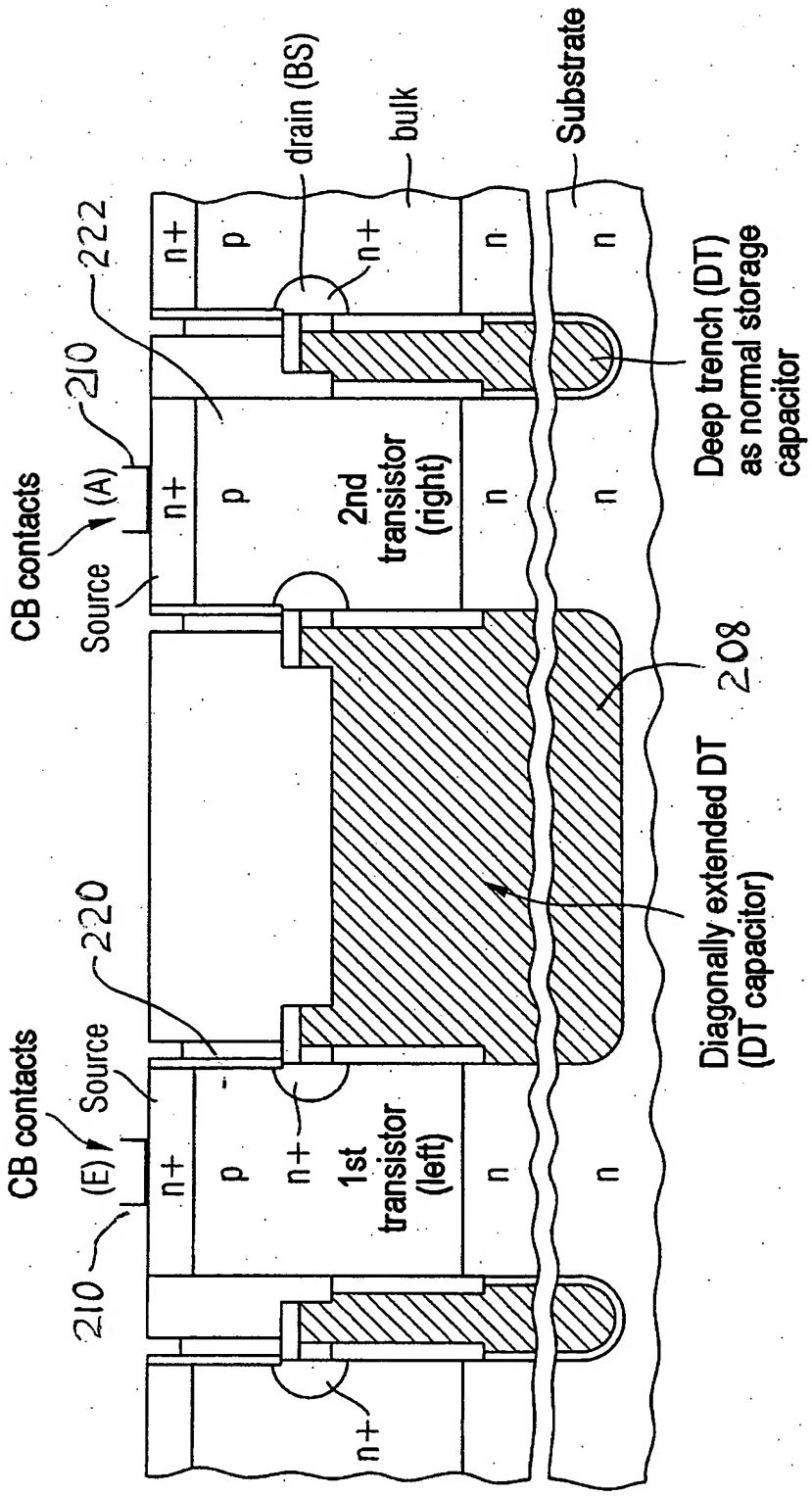

CB contacts
(E)
Source
210
n+
p
n+
1st transistor (left)
n
n
n+
220
CB contacts
Source
(A)
210
222
n+
p
2nd transistor (right)
n
drain (BS)
bulk
n+
n
Substrate
n
Deep trench (DT) as normal storage capacitor
208
Diagonally extended DT (DT capacitor)

FIG 2C

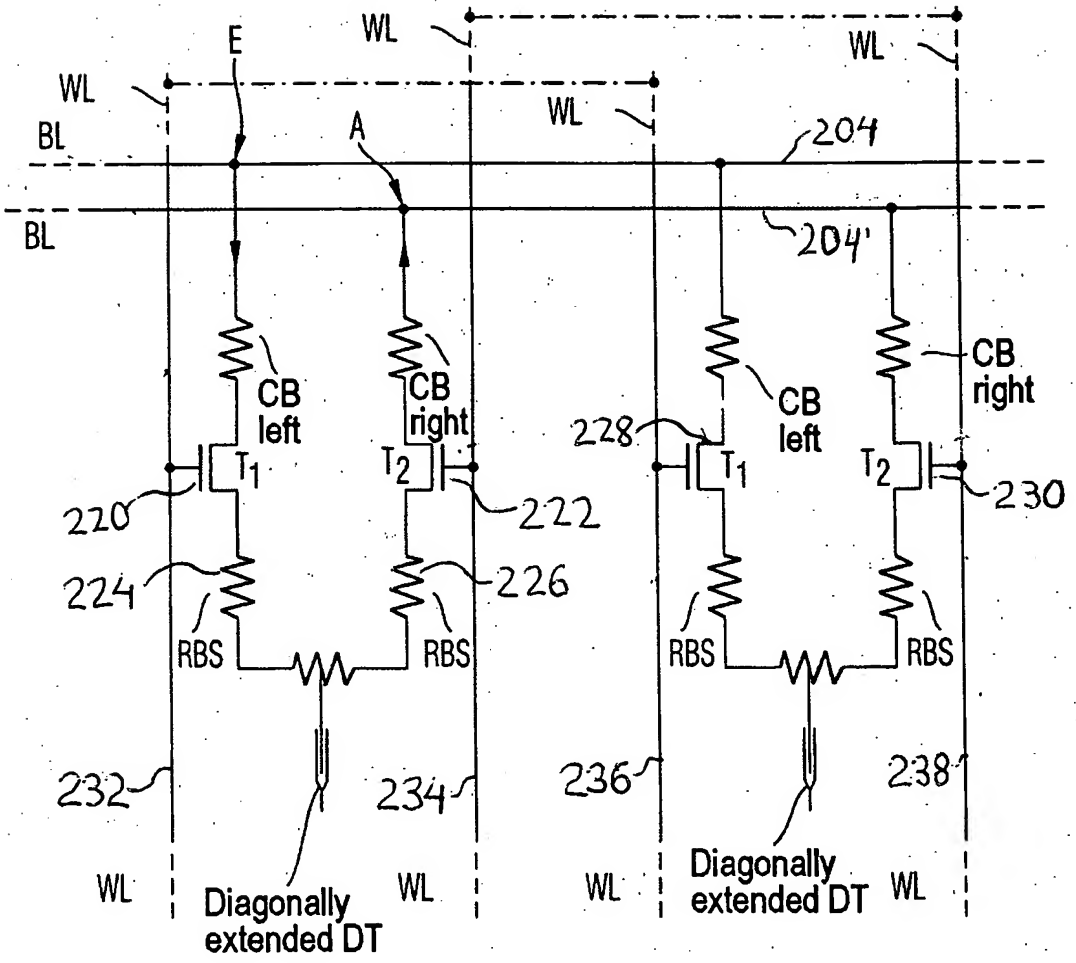

E
WL
WL
WL
WL
BL
A
204
BL
204'
CB left
CB right
CB left
CB right
228
T1
T2
T1
T2
220
222
230
224
226
RBS
RBS
RBS
RBS
232
234
236
238
WL
Diagonally extended DT
WL
WL
Diagonally extended DT
WL

FIG 3A

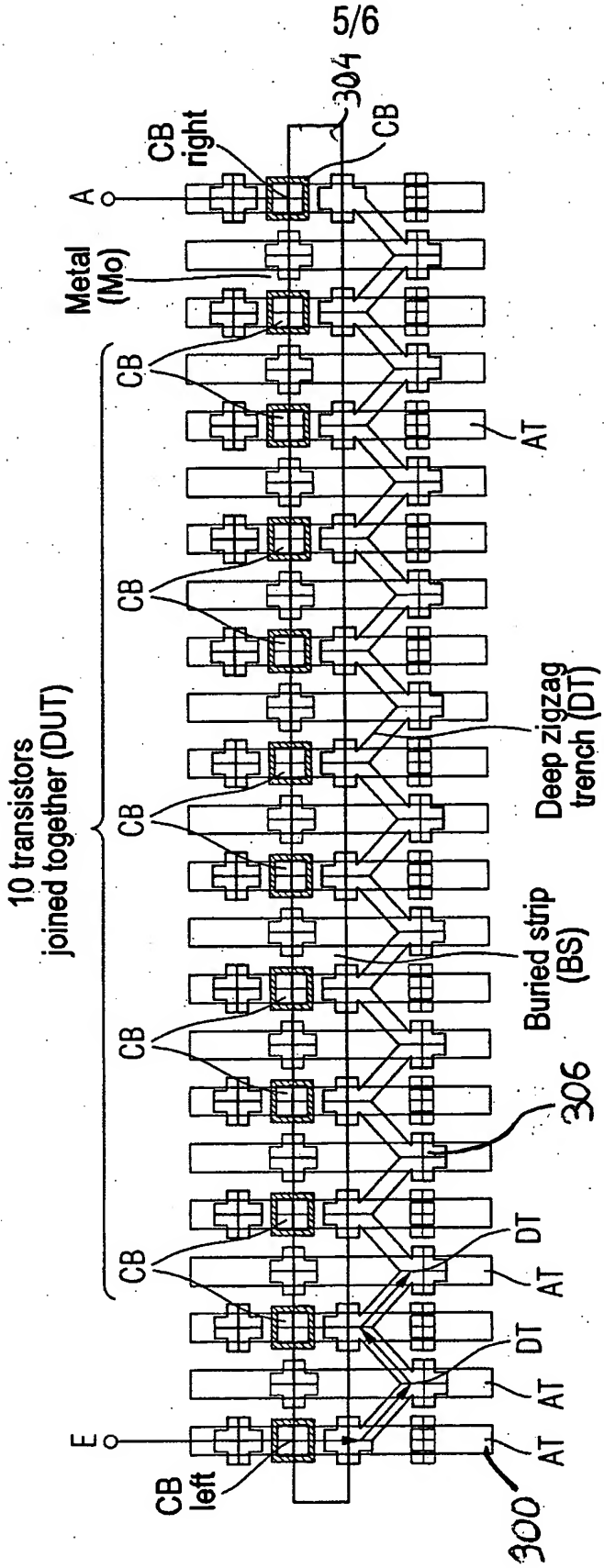
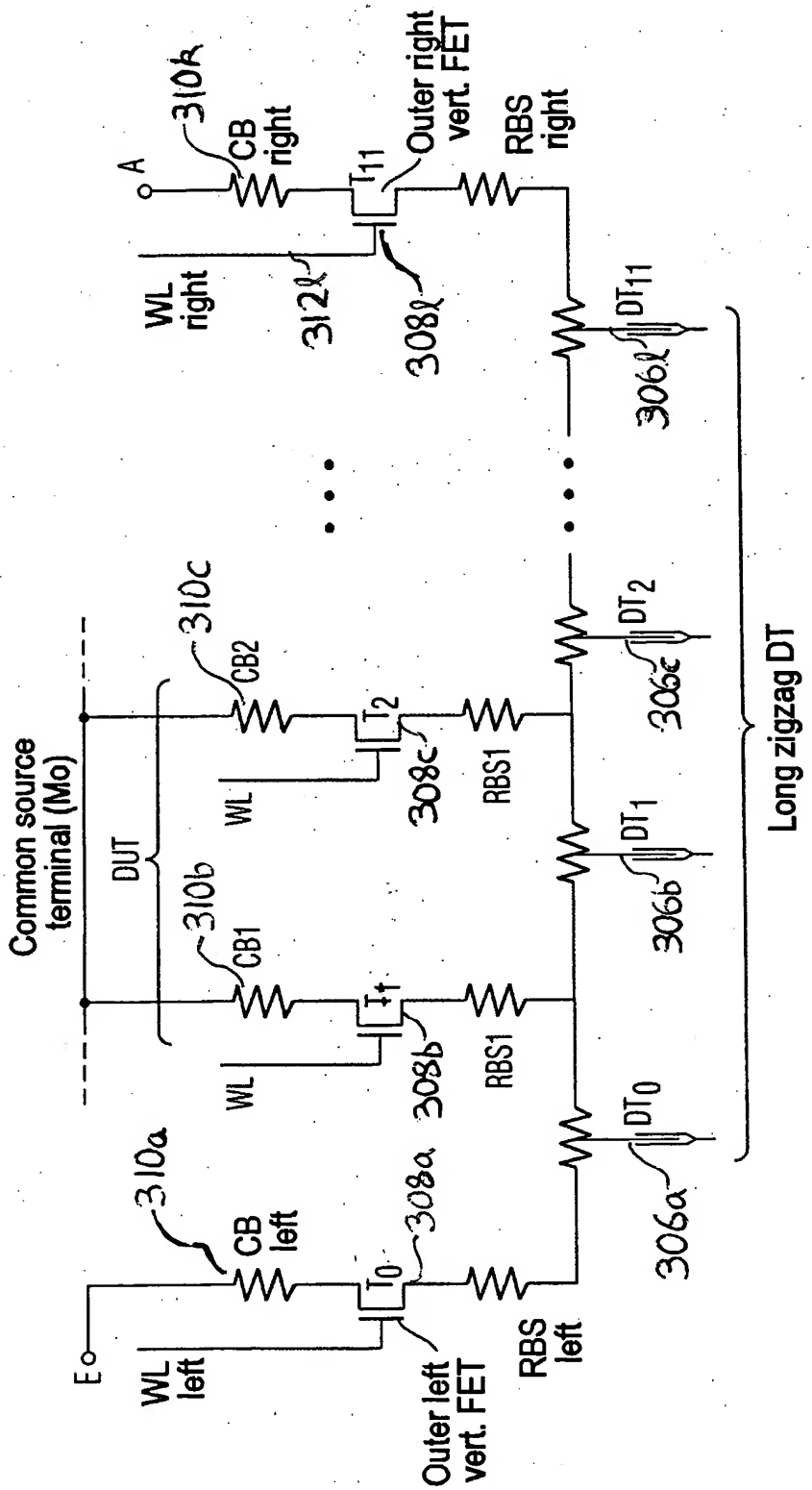

304
CB
CB right
A
Metal (Mo)
CB
AT
CB
CB
10 transistors joined together (DUT)
Deep zigzag trench (DT)
CB
Buried strip (BS)
306
CB
DT
AT
DT
AT
E
AT
CB left
300

FIG 3B


Common source terminal (Mo)
DUT
E
A
WL left
WL right
CB left
CB right
CB1
CB2
310a
310b
310c
310k
WL
WL
WL
312ℓ
Outer left vert. FET
Outer right vert. FET
RBS left
RBS right
RBS1
RBS1
308a
308b
308c
308ℓ
T_0
T_1
T_2
T_{11}
DT_0
DT_1
DT_2
DT_{11}
306a
306b
306c
306ℓ
Long zigzag DT